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(54) Method of using erodable masks to produce partially etched structures in ODE wafer structures.

(57) A thermal ink jet silicon water printhead is formed in a single etching operation by partially etching into one portion of the water (10) while at the same time completely etching through another portion of the water. An erodable mask layer (18) is used to delay formation of the partially etched regions in the water, the depth of the etching being defined by the etch time after the removal of the erodable masking layer, or by the V-groove (14) termination as determined by via opening in a non-erodable mask layer (22).

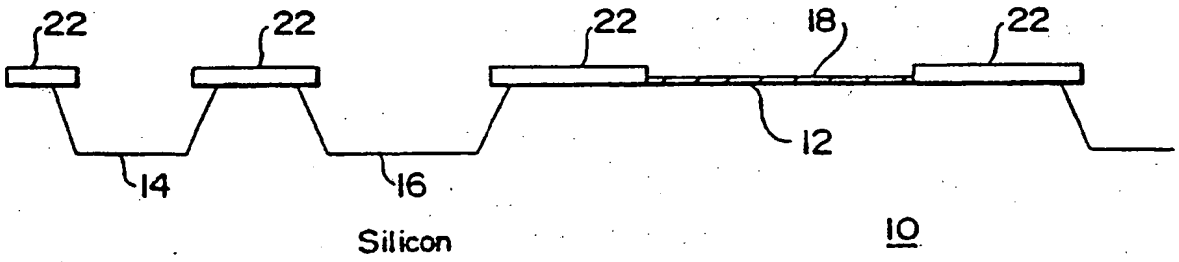

Fig. 2

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METHOD OF USING ERODABLE MASKS TO PRODUCE PARTIALLY ETCHED STRUCTURES IN ODE WAFER STRUCTURES

The invention relates to a method of fabricating an opening in a wafer, more especially a silicon wafer suitable for use in a thermal ink jet printhead.

Thermal ink jet printing is a type of drop- on-demand ink jet printing wherein an ink jet printhead expels ink droplets on demand by the selective application of an electrical pulse to a thermal energy generator, usually a resistive heater, located in capillary-filled, parallel ink channels a predetermined distance upstream from the channel orifices or nozzles. The channel ends opposite the nozzles are in communication with a small ink reservoir to which a larger external ink supply is connected. The printhead normally includes a heater plate on which the heaters are located, and a channel plate in which channels are formed to serve as the above-mentioned ink channels for conveying ink from the ink supply to the resistors for expulsion at the nozzles.

Production of thermal ink jet printheads utilizes the properties of Orientation Dependent Etching in the formation of channels in the channel plate. The wafer, which is preferably silicon, has its major surfaces lying substantially in the "100" plane and internal "111" planes at an angle for silicon of 54.7° to the 100 planes. Openings are formed in the silicon wafer using an anisotropic etchant which works much more normally to the 100 plane than it does laterally or parallel to the 100 plane. Hence, the etchant works less in the 111 planes and thereby leaves inverted pyramidal openings in the wafer. The location of an opening is determined by applying an etch mask to the surface of the wafer to be etched and then opening a via in the mask material through which the etchant can attack the 100 planes. The depth of the opening if etched to termination (i.e., when all exposed 100 planes are removed) is generally a function of the size of the via and the thickness of the wafer. For example, if the via opening, V, in the etch mask M is designed to produce a through-hole H just reaching the opposite side CS of a 20 mil thick silicon wafer (see Fig. 68), it will actually produce a 1.4 mil wide opening 0 on a 19 mil thick wafer W2 (Fig. 6A) and will not produce any opening at all on a 21 mil thick wafer W3 (see Fig. 6C). Decreasing the size of the via opening V (Fig. 6D) will also affect the depth of the cavity since the size of the via determines the area of 100 planes subject to attack. In particular, the depth is defined by the following formula: the depth of the opening equals one-half the product of the smallest via opening dimension and the tangent of 54.7% (for a silicon wafer).

With this technology, it is possible to etch structural patterns in the silicon wafer with close dimensional tolerances. The patterns are formed by through-hole technique (e.g., Figs. 6A and 6B which create a through-hole in the wafer), V-groove termination (e.g., Figs. 6C and 6D which create a V-groove recess of a predetermined depth), or a combination of both. However, it is sometimes useful to produce large etch areas of varying depth that will terminate within the wafer at the same time, and the foregoing technology cannot readily satisfy this need. For example, if a 20 mil silicon wafer is patterned to include a through-opening and a V-shaped groove channel about 46-47 microns deep and about 65 micron wide, it will take about four hours for the etchant (e.g., 30% KOH at 95° C) to form the through-hole, but substantially less time to form the V-groove. For a single etching step operation, the wafer remains in the etchant until the through opening is completed, thus subjecting the V-groove to continued etchant exposure even after the V-groove etch has terminated. The longer the wafer remains in the etchant, the greater the possibility that the etchant will find a crystal defect in the V- groove which it could attack, thus affecting the desired 65 micron channel width.

An object of the present invention is to enable the foregoing disadvantages to be overcome and to provide a method that enables openings of varying depths to be etched in a wafer in a single tch step.

The present invention provides a method which anisotropically etches partially into one portion of a wafer using an erodable mask material. The depth of the partial etching is controlled either by the rate of erosion of the mask material, and/or the thickness of the masking material, so that the desired partial etch depth is obtained upon termination of etchings in the remaining portions of the wafer.

More specifically, the present invention provides a method of fabricating an opening in a wafer comprising the steps of:

applying an erodable first mask to a surface of the wafer;

patterning the erodable first mask to define an erodable first mask layer at a desired location for the opening;

applying a second mask layer over the erodable mask layer;

patterning the second mask layer to expose the erodable first mask layer;

anisotropically etching through the first erodable mask layer and into the wafer to form the opening to a desired depth.

The present invention also provides a method

of fabricating at least two openings of different depths in a wafer, the method of comprising the steps of:

applying an erodable first masking layer to a surface of the wafer;

patterning the erodable first masking layer to form a first via at a desired location for a first opening;

applying a second masking material over the surface of the wafer and the erodable first masking layer;

patterning the second masking layer to expose the first via and form a second via at a desired location for a second opening, the second via exposing the first erodable masking layer;

anisotropically etching the wafer and the erodable masking layer through the first and second vias for a predetermined period of time to form the first opening with a depth greater than a depth of the second opening. The etching of the second opening may terminate at substantially the same time as the etching of the first cavity terminates. The etching of the first opening may terminate when the predetermined period of time expires.

The present invention further provides a method of fabricating at least two openings of different depths in a wafer, the method comprising the steps of:

applying a non-erodable masking layer to a surface of the wafer;

patterning the non-erodable masking layer to form first and second vias at desired locations for first and second cavities, respectively;

applying an erodable masking layer to the surface of the wafer to cover the first and second openings;

patterning the erodable masking layer to expose the wafer surface at the first via;

anisotropically etching the wafer and the erodable masking layer through the first and second vias for a predetermined period of time to form the first opening with a depth greater than a depth of the second opening.

By way of example only, embodiments of the invention will be described with reference to the accompanying drawings in which like reference numerals denote like elements and wherein:

Figures 1-4 are schematic side views of a silicon wafer at different stages of an etching process;

Figure 5 is an enlarged schematic view of a channel plate prior to completion of an etching process; and

Figures 6A-6D are schematic side views of an etched silicon wafer.

A method in accordance with the invention will be described below with reference to a silicon wafer, but is applicable to any type of wafer or substrate capable of orientation dependent etching. The method will also be described with reference to formation of a terrace in a wafer (i.e., a wafer opening having sloping side walls), but is applicable to any etched opening including V-grooves or through-holes. Further, the method will be described in connection with the fabrication of a printhead as disclosed in U.S. Patent RE 32,572, but is applicable to any type of printhead employing a wafer with openings of varying depths.

The method will be described with reference to Figs. 1-4 which illustrate the formation of a terrace 12, V-groove 14 and through-hole 16 in a silicon wafer 10. In Figure 1, a first erodable masking layer 18 has been applied at the desired location for the terrace 12, preferably by applying the first masking layer 18 over the upper surface of the wafer 10 and first masking layer 18 over the upper surface of the wafer 10 and then patterning the erodable mask material to leave the first erodable masking layer 18 at the desired location(s). A second non-erodable masking layer 22 is then applied over the wafer 10 to cover the wafer 10 and the first erodable masking layer 18. The second non- erodable masking material is then patterned to form the desired vias, at least one of which exposes the first masking layer 18. In Figure 1, the second non-erodable masking layer 22 is patterned to include three vias: a first via 12V for the terrace 12, a second via 14V for the V-groove 14, and a third via 16V for the through-hole 16. It is noted that the application of the second non- erodable masking layer 22 may entail some overlap over the edge of the first erodable masking layer 18. Further, it is noted that the erodable masking layer 18 may be applied after application of the non-erodable masking layer 22.

The wafer 10 is then subjected to an etchant. Preferably the etching is a single step process wherein the wafer is subjected to the etchant for a predetermined period of time sufficient to form the deepest opening, (for example the through-hole 16). To etch a through-hole in a 20 mil thick wafer, the predetermined period of time is about 4 hours for 30% KOH at 95° C. The predetermined period of time will vary depending on the type of etchant, the etchant temperature and the etchant concentration.

Figure 2 illustrates the etching process at some period of time less than the predetermined period of time, for example after about 1-2 hours of a 4 hour process (depending on the type, temperature and concentration of the etchant). The wafer has been etched at the second and third vias 14V, 16V, for the V-groove 14 and through-hole 16, respectively, but has not yet attacked the wafer through the first via 12V since the etchant has not yet etched through the erodable first masking layer 18. However, Fig. 2 illustrates that the thickness of the erodable first masking layer 18 has decreased due to th erosion of the first masking layer 18.

Figure 3 illustrates the process at a later time, for example after about 3 hours of the 4 hour process (depending on the type, temperature and concentration of the etchant). In Figure 3, the etching of the V-groove 14 has terminated, but the etching of the through-hole 16 continues. Even though etching of the V- groove 14 has terminated (to a depth in accordance with the formula discussed above), the V-groove 14 will be subjected to continued etchant exposure for the remainder of the etching process (i.e., for about 1 hour depending on the type, temperature and concentration of the etchant). Such continued exposure increases the risk that the etchant will uncover a crystal defect in the V-groove which it could attack, thus affecting the desired width of the V-groove. Figure 3 also illustrates that the etchant has eroded the first masking layer 18 and can now attack the wafer to form the terrace 12. However, the commencement of the wafer etching to form the terrace has been delayed for about three hours due to the presence of the erodable masking layer 18. Thus the terrace 12 will not be exposed to excess etchant exposure since etching of the terrace 12 will continue for only so long as necessary to complete etching of the through-hole 16.

Figure 4 illustrates the wafer at the completion of the etchant proces, e.g., after the 4 hour predetermined period of time, when the wafer is removed from etchant exposure. In Figure 4, the etchant has completely etched through the wafer to form the through- hole 16. However, the depth and width of the terrace 12 are controlled since it was exposed to etchant for less time, thus reducing the risk that crystal defects in the terrace will be uncovered by the etchant. It is noted that etching of the terrace 12 would have continued if the wafer remained exposed to the etchant. Thus, the depth of the terrace can be controlled by controlling the time of exposure to the etchant. The method, however, permits the desired depth of the terrace 12, V-groove 14 and through-hole 16 in a single etching operation without necessarily exposing the terrace to excess etchant exposure while awaiting completion of through-hole etching.

The concepts of Figs. 1-4 are applicable to the V-groove 14 as well. That is, the first masking layer 18 could be applied over the via 14V so that the etchant must first erode the first masking layer 18 before etching the V-groove 14. The timing of the termination of V- groove etching can then be controlled to approximately coincide with the termination of the through-hole etching so that the V-groove 14 would not be exposed to etchant during the time period necessary for completion of the through-hole etching.

The method thus provides a means of producing large areas on a silicon wafer that are partially etched into the wafer while at the same time other portions of the wafer are completely etched through. This is accomplished by using a mask, in the areas to be partially etched through, of a material that slowly erodes away in the silicon etchant. The depth of the terrace structure can be controlled by the size of the via (by the formula discussed above) in conjunction with control of either the rate the mask erodes or the thickness of the masking material or a combination of both. Silicon Dioxide is a prime example of an erodable mask, having an etch rate in 30% KOH at 95°C of approximately 1 um/hr for thermal oxide and 8.4 um/hr for LOTOX, 4% PSG. For very deep terraces the LOTOX masking material would be appropriate while the thermal oxide would be appropriate for shallower terraces. For ODE structures making use of highly doped layers as an etch stop where EDP is the etchant, a nitride masking layer could be used since nitride etches at a rate of 60 um/hr and very thin layers of nitride are known to be a very effective etch resistant layer(s).

The described method is applicable to the production of a thermal ink jet printhead having an etched channel plate 31 (schematically illustrated in Fig. 5 as the area within dice lines 13). The channel plate 31 includes, among other things, a plurality of through etched feed holes 24, two shallow V- groove reservoirs 42 adjacent the end feed holes 24, and a plurality of ink channel recesses 20. One end of the channel recesses 20 is diced along dice line 13 to form nozzles, and the opposite end communicates with the feed holes 24 and V-groove reservoirs 42. Figure 5 illustrates the channel plate 31 prior to completion of the etching for the through holes 24, which include 111 plane sidewalls 245 and 100 plane floor or bottom 24B.

The optimum channel recess size for the channel recesses 20 is normally about 46-47 microns deep and 65 microns across. In a single etch operation, the channel recesses 20 would terminate well prior to the time for termination of etching for the feed holes 24. Accordingly, the channel recesses 20 would be exposed to etchant while waiting for the termination of the feed hole etching, thus increasing the risk of the etchant uncovering a crystal defect in the recess 20 which the etchant could attack, thus resulting in a potential variation in recess width. To obviate this potential disadvantage, the first erodable masking layer 18 could be applied and patterned at the locations for the channel recesses 20, and the second non-erodable masking layer 22 could then be applied and patterned to expose the first erodable masking layer and the vias for the feed holes 24 and shallow recesses 42 in a manner similar to that described with references to Figs. 1-4. Depending on the erodable masking material, size of the vi a, and the

time of etchant exposure, the depth of the channel recess can be controlled by controlling the rate of erosion of the erodable mask layer and/or the thickness of the erodable mask layer. Further, the time of termination of the etching for the channel recess 20 can be controlled by controlling the erosion rate and/or thickness of the erodable mask layer, so that the desired channel depth is obtained upon completion of the etching for the feed holes 24. Figure 5 illustrates etching of the channel plate 31 at a point in time comparable to Fig. 3 wherein the etching of the V-grooves 42 is completed, etching of the feed holes 24 is continuing, ad etching of the channel recesses 20 is just beginning since the etchant has removed the erodable masking layer.

Claims

1. A method of fabricating an opening (12) in a wafer (10), the method comprising the steps of applying two masks (18,22) to a surface of the wafer, a first one (18) of the masks being an erodable mask; patterning the masks so that the erodable mask defines an erodable layer at a desired location for the opening, and so that the second mask (22) exposes the erodable layer; and anisotropically etching through the erodable layer and into the wafer to form the opening to a desired depth.

2. A method as claimed in claim 1, in which the applying and patterning steps comprise
applying the erodable mask to the wafer;
patterning the erodable mask to define the erodable layer;
applying the second mask over the erodable mask; and
patterning the second mask to expose the erodable layer.

3. A method as claimed in claim 1 or claim 2, further comprising the step of controlling the depth of the opening by controlling the erosion rate and/or the thickness of the erodable layer.

4. A method of fabricating at least two openings (12, 14, 16) of different depths in a wafer (10), the method of comprising the steps of:
applying an erodable first masking layer (18) to a surface of the wafer;
patterning the erodable first masking layer to form a first via (14V, 16V) at a desired location for a first opening (14,16);
applying a second masking material (22) over the surface of the wafer and the erodable first masking layer;
patterning the second masking layer to expose the first via and lorm a second via (12V) at a desired location for a second opening (12), the second via exposing the first erodable masking layer;
anisotropically etching the water and the erodable masking layer through the first and second vias for a predetermined period of time to form the first opening with a depth greater than a depth of the second opening.

5. A method of fabricating at least two openings of different depths in a wafer, the method comprising the steps of:
applying a non-erodable masking layer to a surface of the water;
patterning the non-erodable masking layer to form first and second vias at desired locations for first and second cavities, respectively;
applying an erodable masking layer to the surface of the water to cover the first and second openings;
patterning the erodable masking layer to expose the water surface at the first via;
anisotropically etching the water and the erodable masking layer through the first and second vias for a predetermined period of time to form the first opening with a depth greater than a depth of the second opening.

6. A method as claimed in claim 4 or claim 5, wherein the etching of the second opening (12) terminates at substantially the same time as the etching of the first opening terminates.

7. A method as claimed in any one of claims 4 to 6, wherein the first opening is a through hole (16).

8. A method as claimed in any one of claims 4 to 7, further comprising the step of controlling the depth of the second opening by controlling the erosion rate and/or the thickness of the erodable layer.

9. A method as claimed in any one of the preceding claims, wherein the erodable mask layer is silicon dioxide.

10. A method as claimed in any one of claims 1 to 8, wherein the erodable mask layer is a nitride masking layer.

11. A channel plate for a thermal ink jet printh ad, having openings fabricat d therein by a method as claimed in any one of the preceding claims.

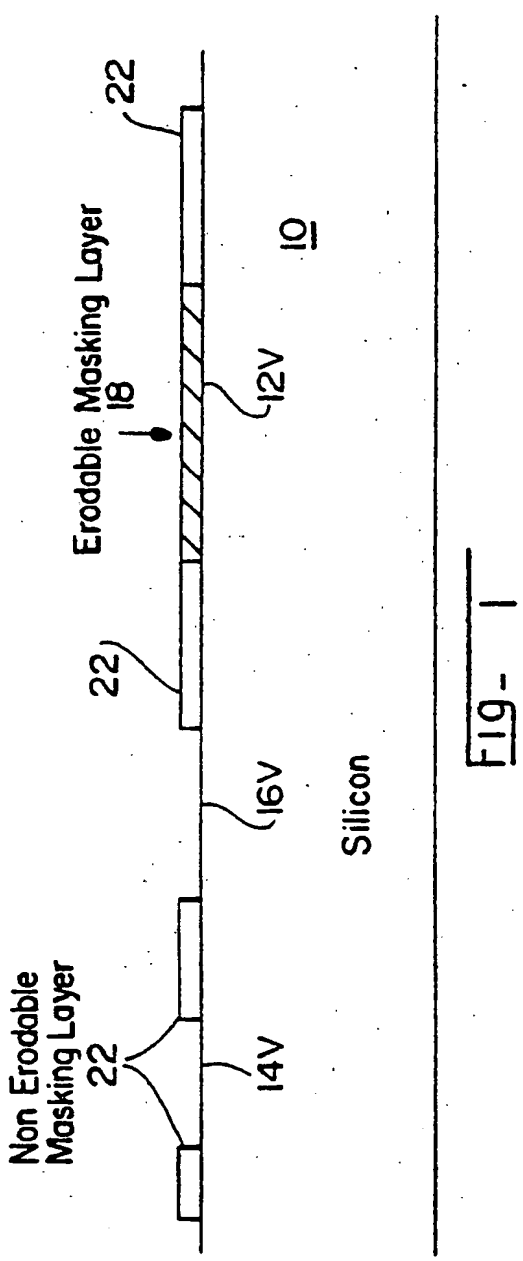

FIG- 1

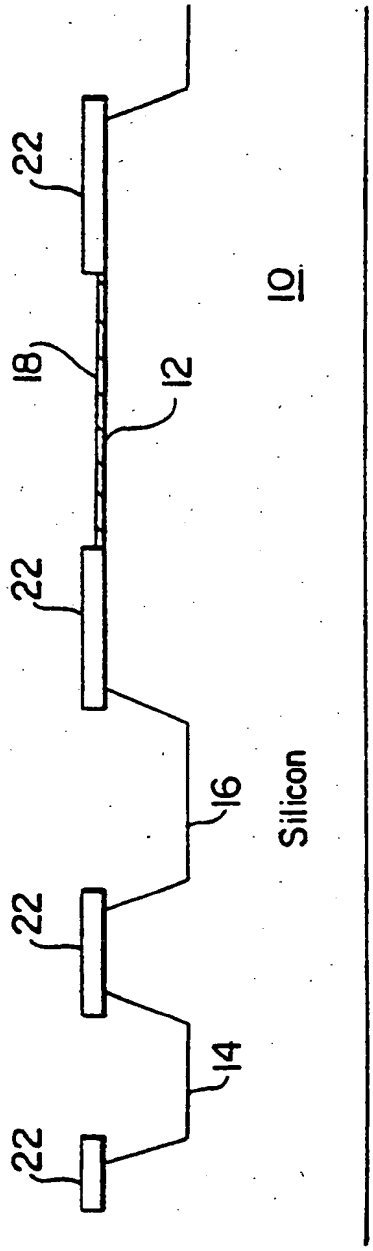

FIG- 2

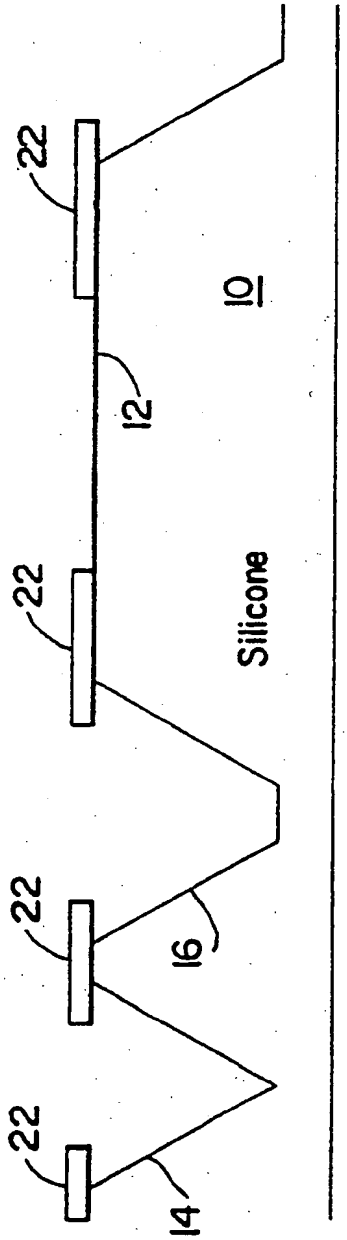
22
22
22
22
10
12
16
14
Silicone

Fig- 3

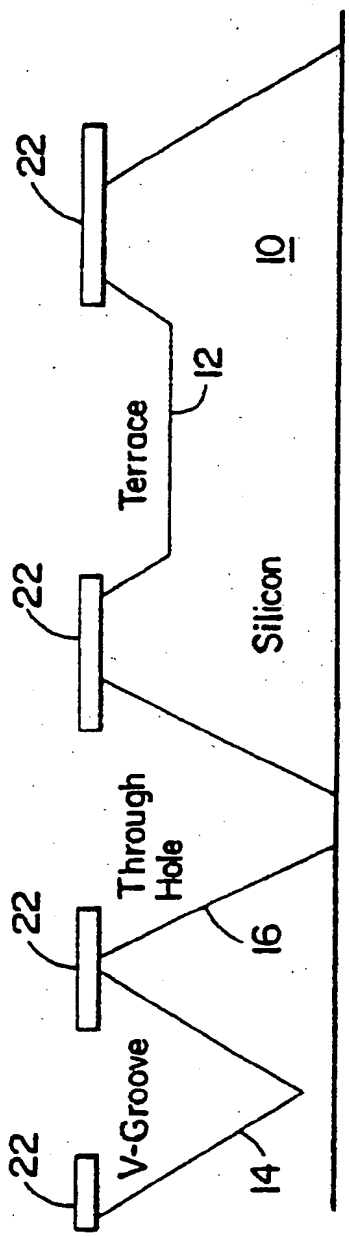
22
22
22
22
10
12
Terrace
Through Hole
16
14
V-Groove
Silicon

Fig- 4

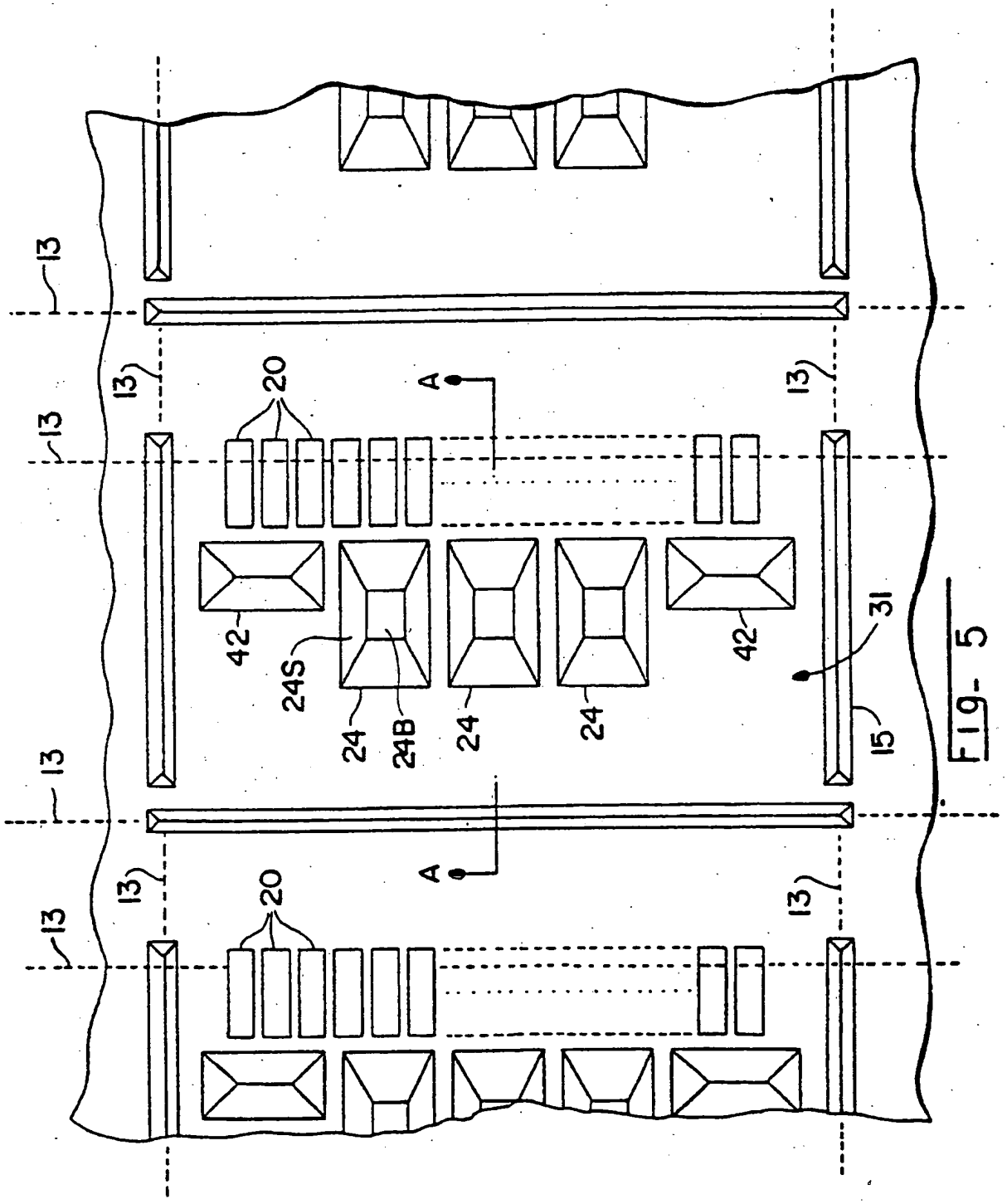

FIG- 5

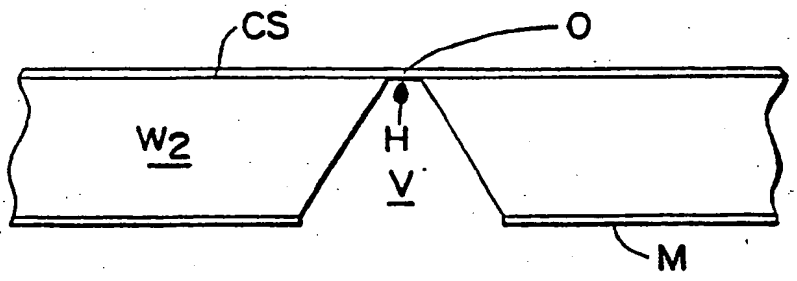

Fig- 6A

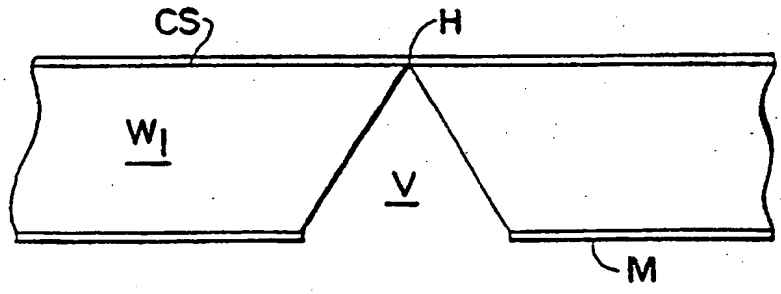

Fig - 6B

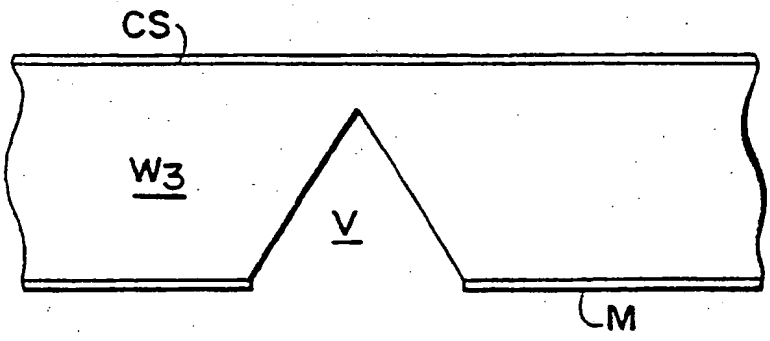

Fig- 6C

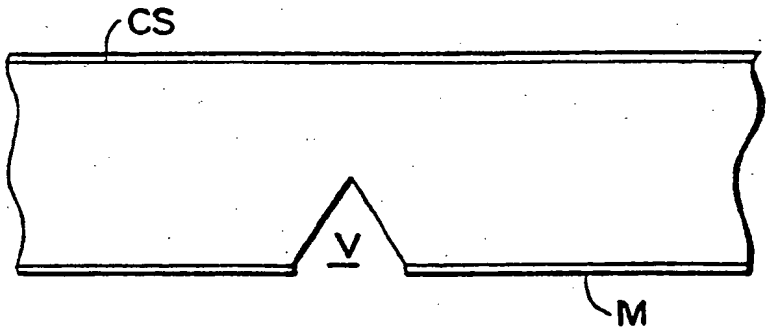

Fig- 6D

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 90314009.3

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	CH - A5 - 614 070 (IBM) * Abstract; fig. 1-8 *	1	G 01 D 15/18 H 01 L 21/467
A	GB - A - 1 407 861 (WESTERN ELECTRIC) * Fig. 2 *	1	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G 01 D 15/00
H 01 L 21/00

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	21-03-1991	KUNZE

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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